CHIPSID PRODUCT ANALYSIS TEST REPORT

SCOPE

chipsID employs the SAE AS6171 Revision A standard as a framework for conducting counterfeit mitigation inspections. However, it is important to note that chipsID does not strictly adhere to this standard as a mandatory requirement for inspections. Instead, the inspection test plan is tailored selectively according to each customer's specific requirements. chipsID's counterfeit inspection services presently focus exclusively on active complex and active simple components due to their heightened susceptibility to counterfeiting, as they are frequently targeted commodities.

REQUIREMENT

chipsID places significant importance on the quality of its inspection reports. To ensure accurate and high-level confident comparisons, it is mandatory for all customers to provide a golden sample reference for inspection purposes. If a golden sample is already available in chipsID's database or has been previously provided, it will be utilized for comparison. chipsID will not proceed with the inspection unless a golden sample reference is available. The suspected counterfeit detection sequence has been established based on inspection and testing of parts by selecting the least costly inspections that are most effective, and easiest to perform first, and then to build upon results of previous testing in accordance with the sequence to build confidence in the results. All test data and test reports supplied to the Requester shall be retained by chipsID for a minimum of 5 years, or longer if specified by agreement with the Requester, in a manner to protect against damage from fire, flood, and other environmental hazards.

Note: In this test report, the term "golden sample" refers to a Known Good Device (KGD) obtained either directly from the Original Component Manufacturer (OCM) or from the authorized distribution channel, accompanied by Chain of Custody documents to ensure traceability.

chipsID Product Analysis Test Report Rev. A

Customer Name:	XXXXXXXX
Purchase Order:	Sample Test Report
Inspection Date:	

Disclaimer

chipsID is dedicated to ensuring the highest standard of product testing in the industry and extend every effort to report reliable data and an accurate interpretation. By utilizing our services, you acknowledge and agree that chipsID shall not be held liable for any direct, indirect, incidental, special, consequential, or exemplary damages, including but not limited to, damages for loss of profits, goodwill, use, data, or other intangible losses resulting from the use or inability to use our services, the cost of procurement of substitute goods and services resulting from any goods, data, information, or services purchased or obtained or messages received or transactions entered into through or from our services, unauthorized access to or alteration of your transmissions or data, statements or conduct of any third party on our services, any other matter relating to our services. In no event shall chipsID be liable for any damages whatsoever arising out of or in connection with the use or performance of our services.

Customer Contact Info:	XXXXXXXX
PO Quantity:	2

Part Information			
Part Number:	MD2001FX	**Customer Internal P/N**	NA
Manufacturer:	ST MICROELECTRONICS	**MSL**	1
Description:	TRANS NPN 700V 12A ISOWATT-218FX	**Lifecycle**	ACTIVE
Complexity per AS6171A	☐Active Complex ☒Active Simple		

Lot Information								
Samples	**Lot Code**	**Date Code**	**COO**	**RoHS**	**Lead Finish**	**Qty.**	**Acceptable**	**Suspect Counterfeit**
Reference/Golden Sample: (Available on chipsID.com)	NA from Customer	NA from Customer	South Korea	RoHS3 Compliant	Matte Tin (Sn)	1		
Sample 1:	Unknown	Unknown	Morocco	Unknown	Matte Tin (Sn) from test.	1	☐	☒
Sample 2:	NA	NA	NA	NA	NA	NA	☐	☐
Sample 3:	NA	NA	NA	NA	NA	NA	☐	☐

Inspection Approval			
Prepared By:	[redacted]	**Job Title:**	Staff Component/Reliability Engineer
Signature:		**Signed Date:**	
Approved By:	[redacted]	**Job Title:**	Sr. Principal Component Quality Engineer
Signature:		**Signed Date:**	

Inspection Test Plan					
AS6171 Inspection Slash Sheet (See DEFINITIONS Section for details)	**Completed**	**Not Completed**	**Not Applicable**	**Qty.**	**Engineering Notes**
PCN Notification	☒	☐	☐	NA	No PCNs found regarding site assembly or die change for P/N MD2001FX from ST Micro.
Packaging and Documentation	☒	☐	☐	2	Packaging is secure with sufficient bubble wraps and proper ESD pink poly bag for the devices.
AS6171/2 – External Visual **Part Dimensions** **Solvent Remarking** **Solvent Resurfacing**	☒	☐	☐	2	Inconsistency in dimensions due to different external package construction.
AS6171/3 – XRF	☒	☐	☐	2	Consistent with golden sample.
AS6171/4 – Decapsulation	☒	☐	☐	2	Inconsistent against golden sample using detailed visual comparison
AS6171/5 – X-ray	☒	☐	☐	2	Inconsistent against golden sample.
AS6171/6 – Acoustic Microscopy	☐	☐	☒	NA	

Inspection Test Plan					
AS6171/7 – Electrical Test	☒	☐	☐	2	Inconsistent against golden sample using Tektronix Curve Tracer 370A
AS6171/8 – Raman Spectroscopy	☐	☐	☒	NA	
AS6171/9 – FTIR Spectroscopy	☐	☐	☒	NA	
AS6171/10 – Thermogravimetric	☐	☐	☒	NA	
AS6171/11 – Design Recovery	☐	☐	☒	NA	

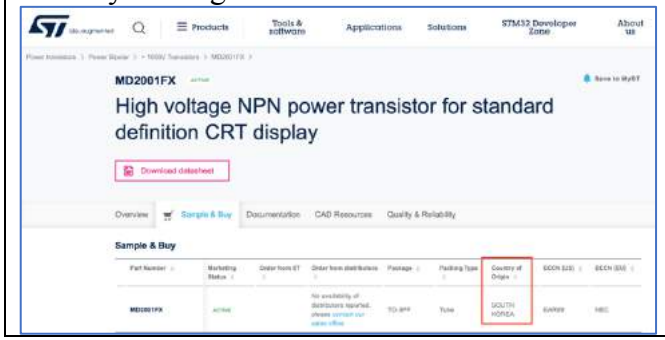
Note: While AS6171 Inspection Slash Sheets are numbered sequentially, the testing conducted progresses from non-destructive to destructive methods.

Inspection Summary

The device under test (DUT), NPN transistor from ST Microelectronics, provided by XXXXXXXX deemed to be a suspect counterfeit device due to multiple inconsistencies. Starting with past PCNs, ST Microelectronics never produces this part in Morocco as indicated on the top marking of the DUT. The only Country of Origin (COO) is South Korea as shown on the website. The overall package of the DUT showed many discrepancies from the physical construction to variation in dimensions. [redacted]

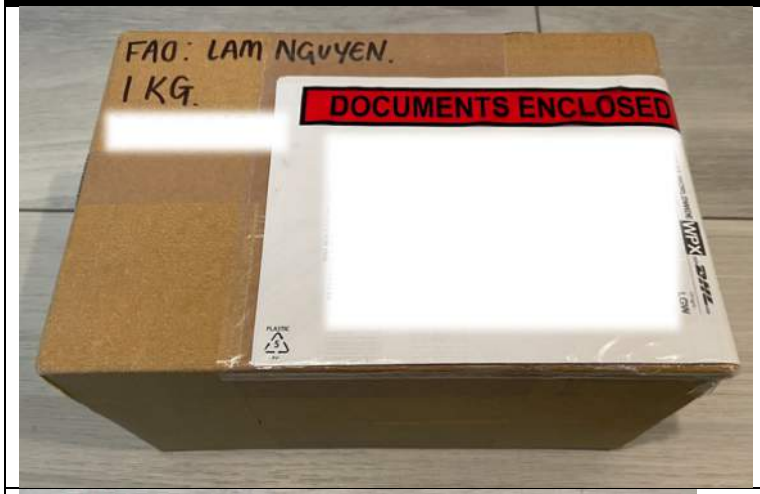
[redacted]

Country of Origin:



The following pages are photos of the part detection test methods for the selected AS6171 Slash Sheet Test Plan by the customer.

INCOMING PACKAGING

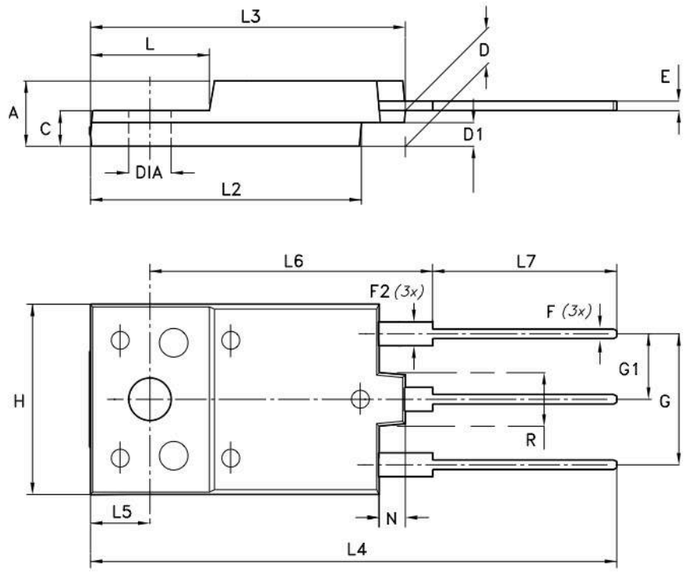


Customer Name:	XXXXXXXX
Purchase Order:	Sample Test Report
Inspection Date:	

AS6171/2 EXTERNAL VISUAL INSPECTION (EVI)

TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS

MECHANICAL DATA FROM DATASHEET



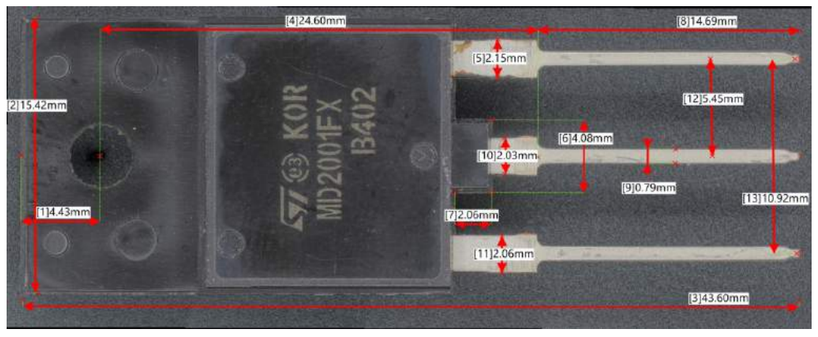
7627132 B

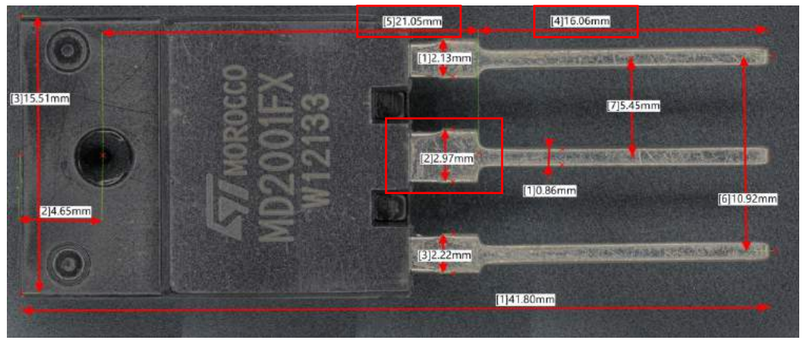
ISOWATT218FX mechanical data

Dim.	mm.		
	Min.	Typ	Max.
A	5.30		5.70
C	2.80		3.20
D	3.10		3.50
D1	1.80		2.20
E	0.80		1.10
F	0.65		0.95
F2	1.80		2.20
G	10.30		11.50
G1		5.45	
H	15.30		15.70
L	9		10.20
L2	22.80		23.20
L3	26.30		26.70
L4	43.20		44.40
L5	4.30		4.70
L6	24.30		24.70
L7	14.60		15
N	1.80		2.20
R	3.80		4.20
Dia	3.40		3.80

DIMENSIONS TOP VIEW

Equipment Used:
Keyence VHX-7000
Digital Microscope





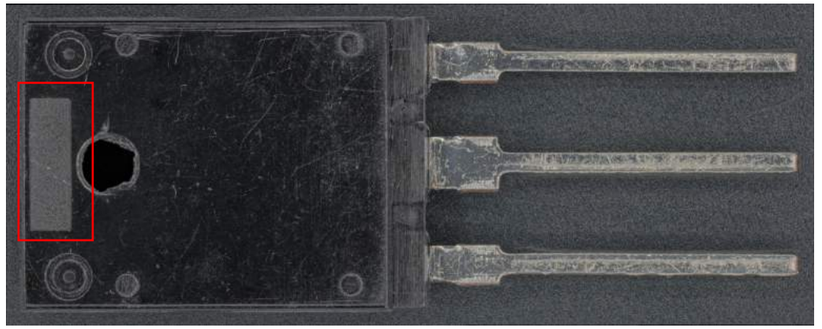
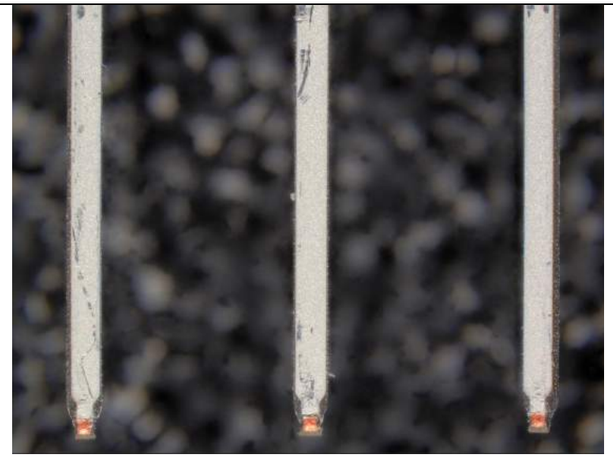
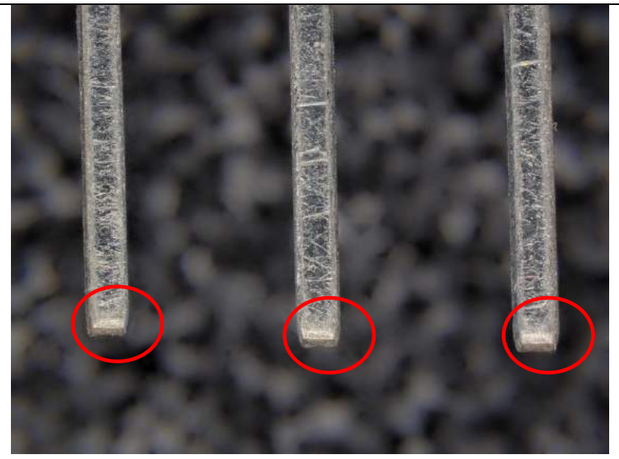
- Top view of the DUT shows significant differences with regards to part markings and overall body construction from the golden sample.

- Inconsistent font type and text alignment between the two devices.

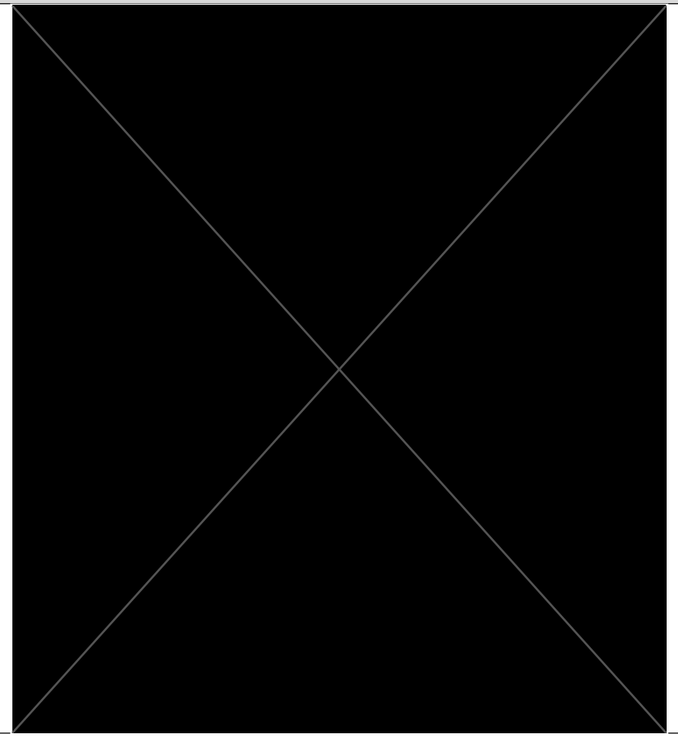
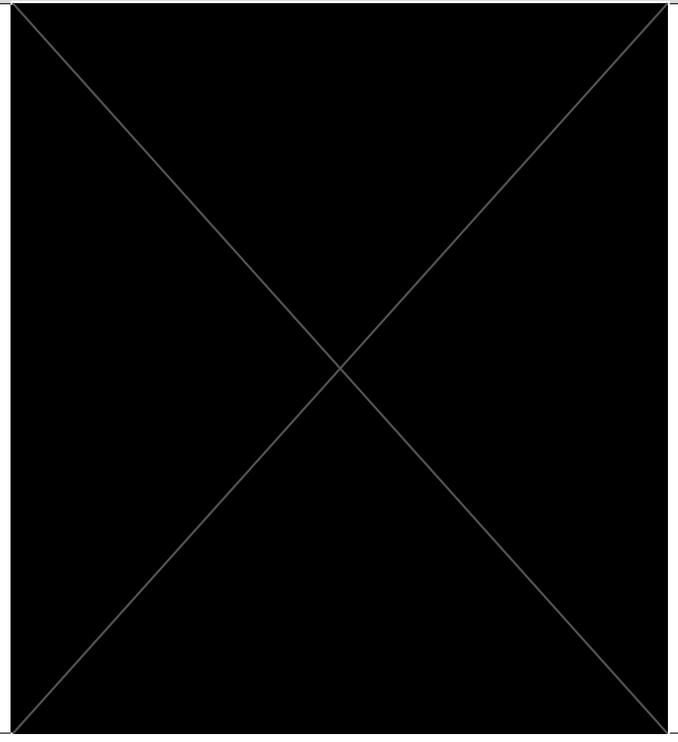
- Inconsistent surface texture between the two devices.

- Upon finding 3 inconsistent measurements of the DUT per datasheet for Dim R, L6, L7.

AS6171/2 EXTERNAL VISUAL INSPECTION (EVI)

TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS
OPTICAL BOTTOM VIEW **Equipment Used:** Keyence VHX-7000 Digital Microscope			- Leads formation of the DUT is inconsistent with the golden sample. - Coating of the leads of the DUT has a shinier look rather than matte finished appearance from the golden sample. - Molding compound of the bottom view shows different injection molding gate locations from the golden sample (and datasheet).
OPTICAL LEADS **Equipment Used:** Keyence VHX-7000 Digital Microscope			- The tips of the leads have inconsistent formation than the golden sample. - Traces of copper shown at the tips for the DUT device but not as clarity and evident as the golden sample

AS6171/2 EXTERNAL VISUAL INSPECTION (EVI)

TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS
REMARKING SOLVENCY TEST [redacted]			[redacted]

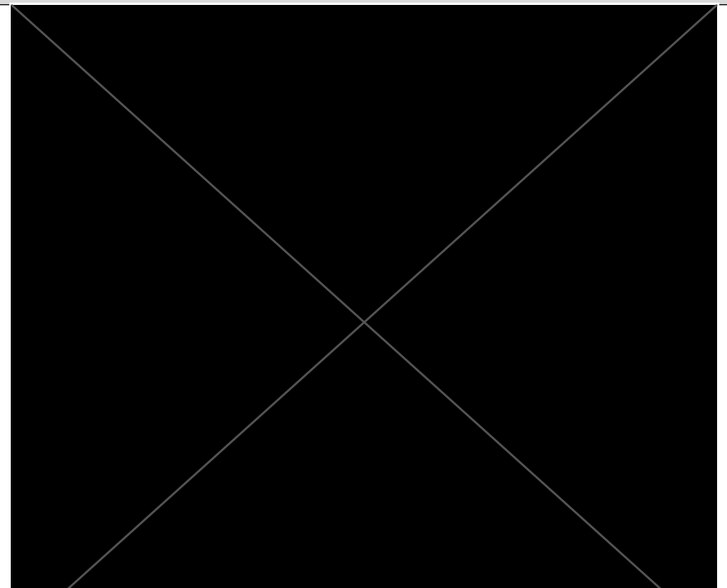
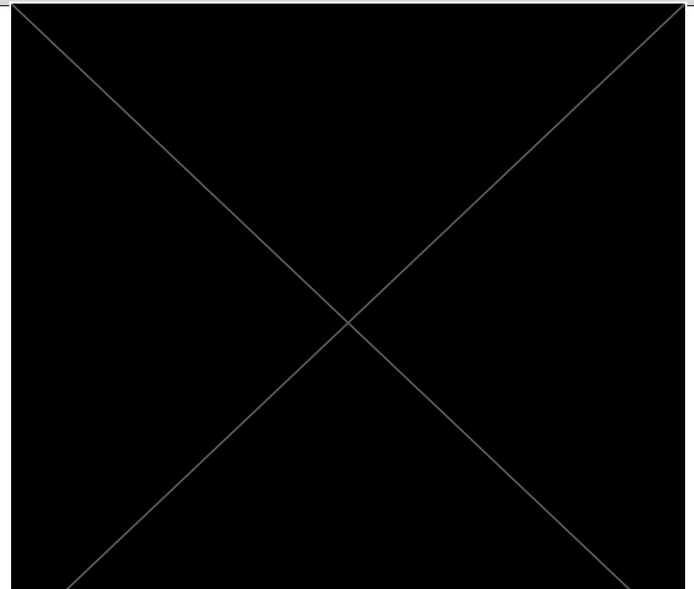
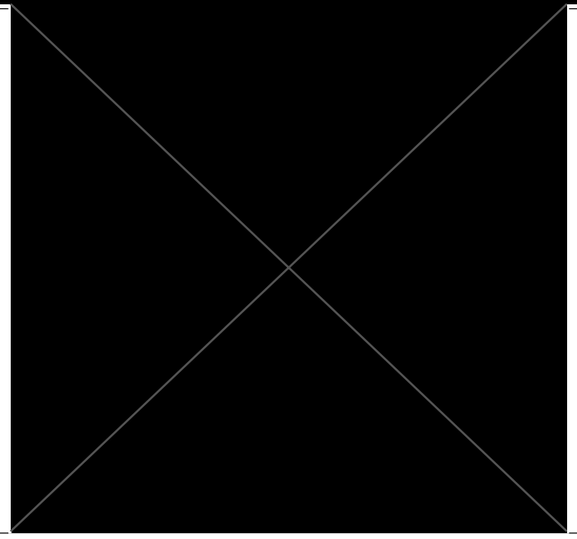
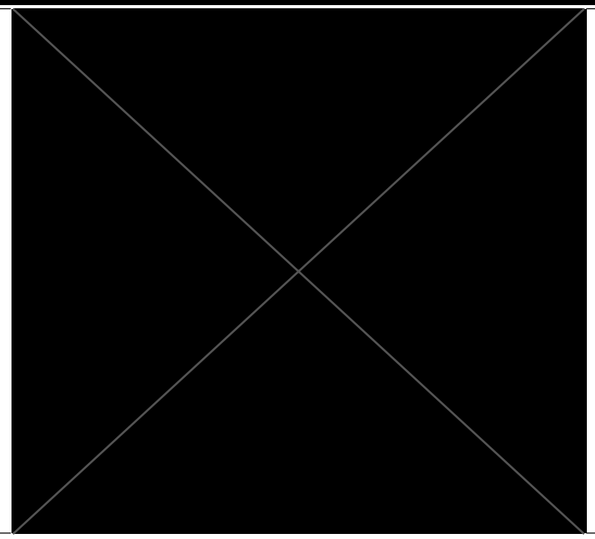
AS6171/2 EXTERNAL VISUAL INSPECTION (EVI)

TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS
RESURFACING ACETONE [redacted]	[redacted]	[redacted]	[redacted]
RESURFACING 1-METHYL 2-PYRROLIDINONE [redacted]	[redacted]	[redacted]	[redacted]

AS6171/2 EXTERNAL VISUAL INSPECTION (EVI)

TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS
RESURFACING DYNASOLVE 750 [redacted]	[redacted]	[redacted]	[redacted]

AS6171/7 ELECTRICAL TEST

TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS
FORWARD VOLTAGE (VF) BASE TO COLLECTOR			
FORWARD VOLTAGE (VF) BASE TO EMITTER			

AS6171/7 ELECTRICAL TEST

TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS
ELECTRICAL RATINGS FROM DATASHEET **V(CES) Collector-Emitter Voltage (VBE = 0)**	MD2001FX Electrical ratings **1 Electrical ratings** **Table 2. Absolute maximum rating** Symbol: V_{CES} — Parameter: Collector-emitter voltage (V_{BE} = 0) — Value: 1500 — Unit: V		
CURVE TRACE	[redacted]	[redacted]	[redacted]

AS6171/7 ELECTRICAL TEST

TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS

ELECTRICAL RATINGS FROM DATASHEET

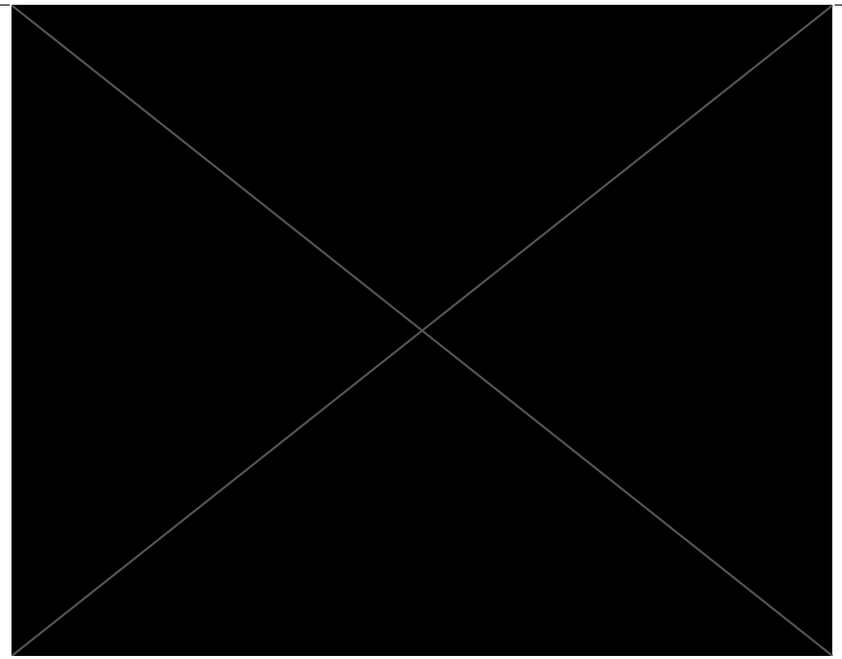
I(CES) Collector Cut-off Current (VBE = 0)

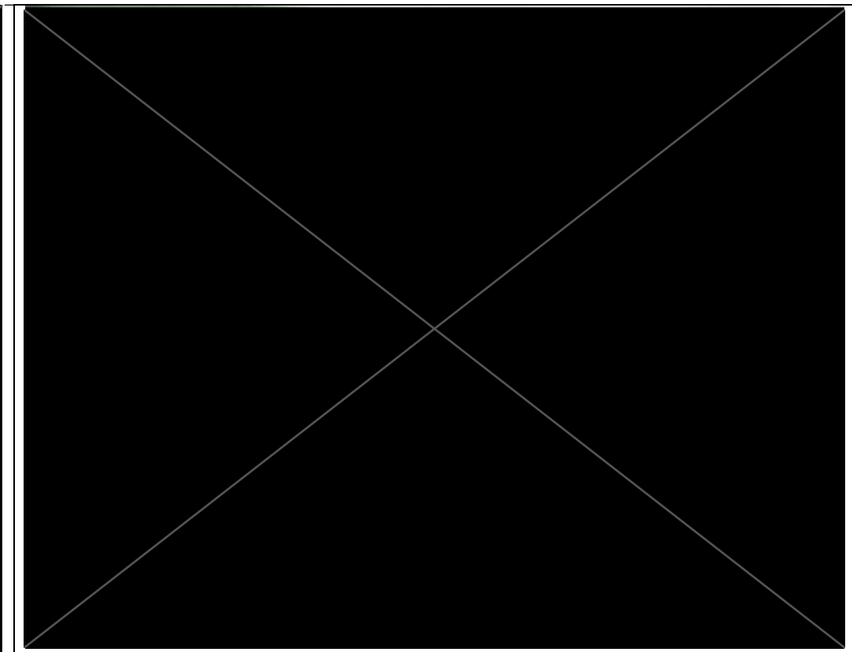
(T_{case} = 25°C unless otherwise specified)

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{CES}	Collector cut-off current (V_{BE} =0)	V_{CE} = 1500V			0.2	mA
		V_{CE} = 1500V; T_C= 125°C			2	mA

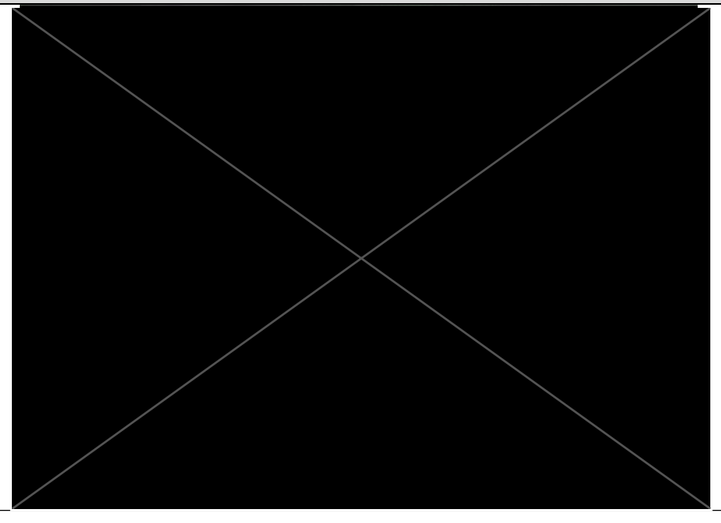
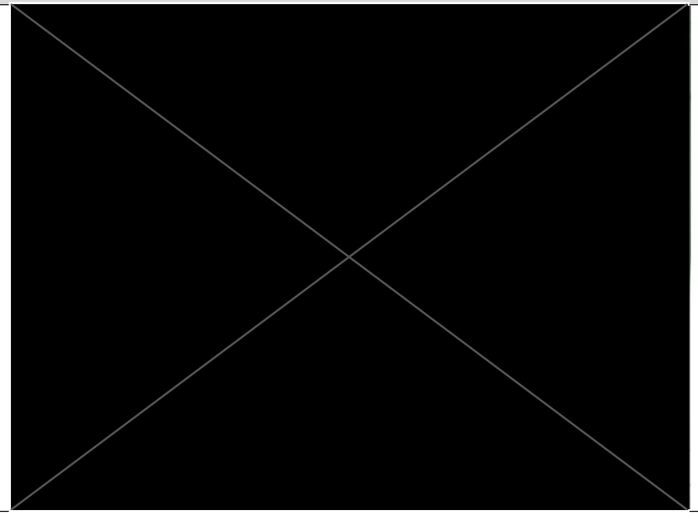
CURVE TRACE



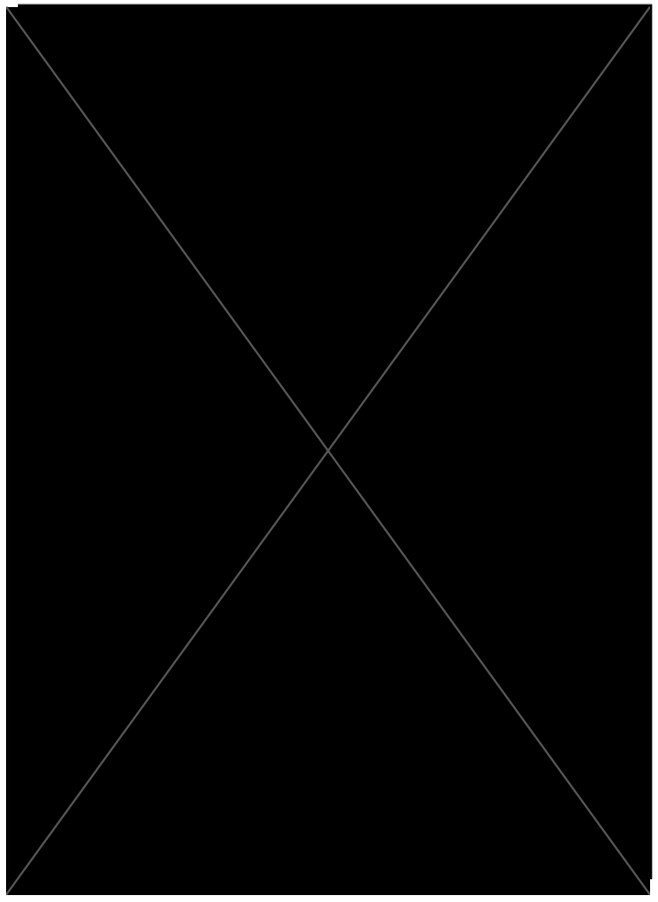
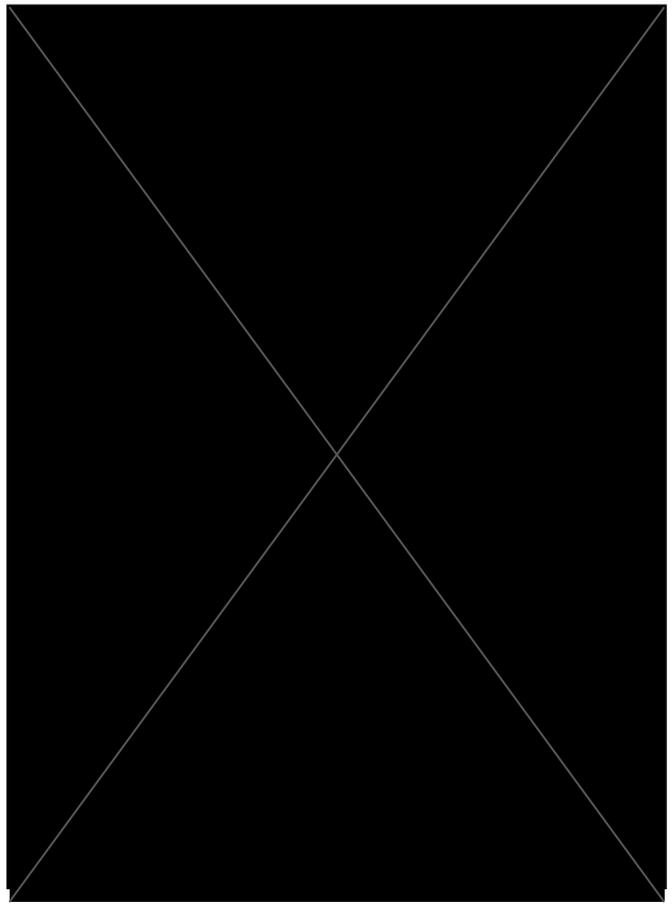


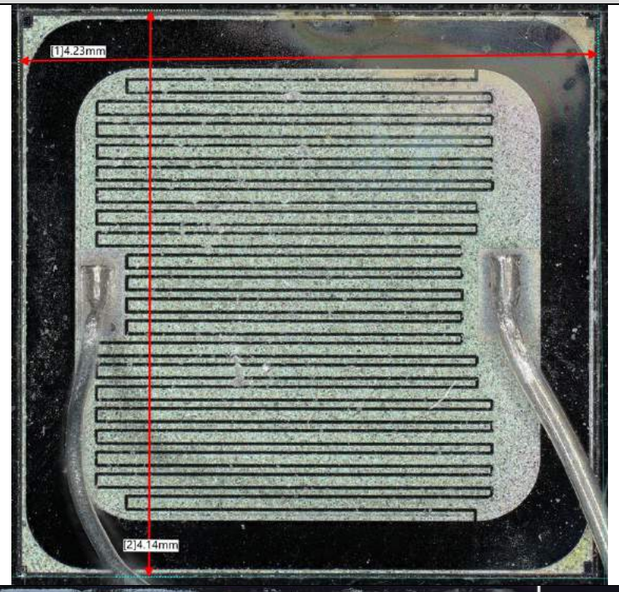
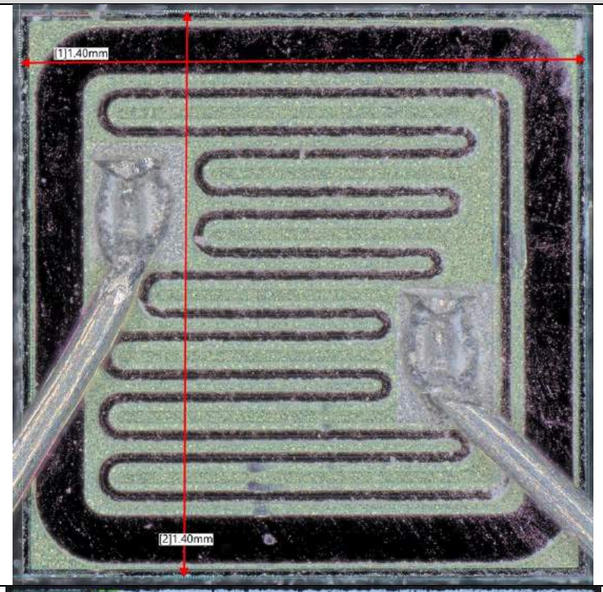
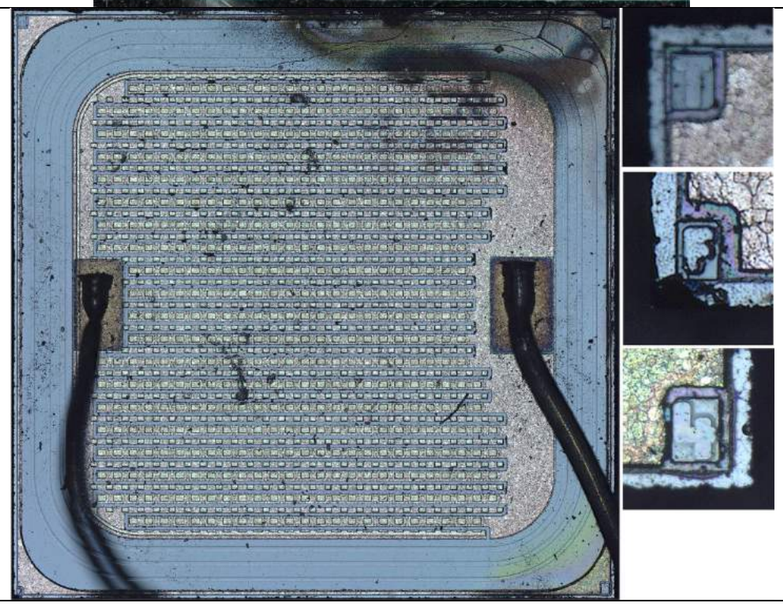
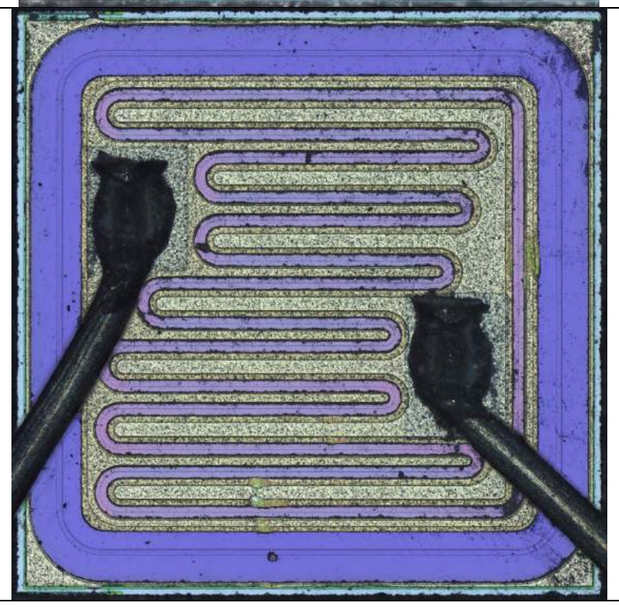
Customer Name:	XXXXXXXX
Purchase Order:	Sample Test Report
Inspection Date:	

AS6171/7 ELECTRICAL TEST

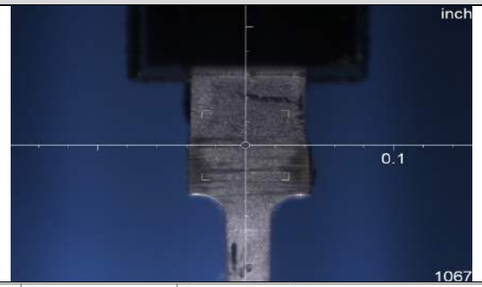
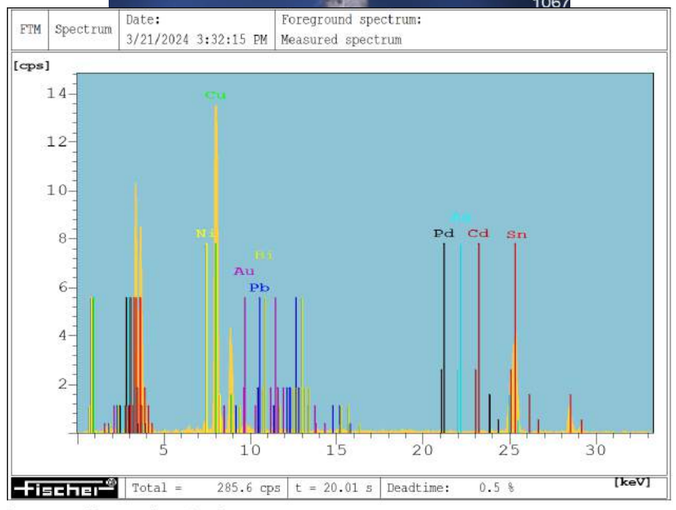
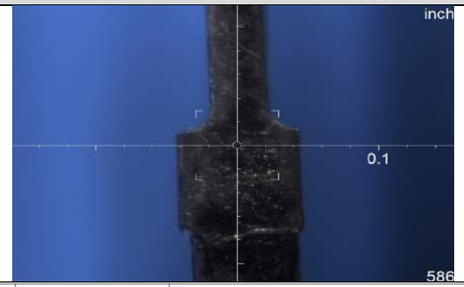
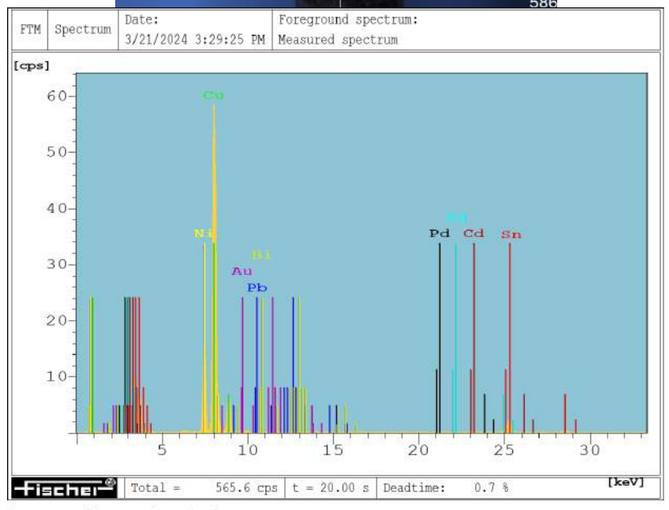
TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS
CURVE TRACE			

AS6171/5 RADIOLOGICAL (X-RAY) INSPECTION

TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS
RADIOLOGICAL (X-RAY) TOP VIEW			

AS6171/4 DELID / DECAPSULATION PHYSICAL ANALYSIS (DDPA)			
TEST METHOD	**REFERENCE / GOLDEN SAMPLE**	**DEVICE UNDER TEST (DUT #1)**	**COMPONENT ENGINEER COMMENTS**
DELID / DECAPSULATION PHYSICAL ANALYSIS (DDPA) **Mixed Lighting** (Dark Field) [redacted]			[redacted]
DELID / DECAPSULATION PHYSICAL ANALYSIS (DDPA) **Coaxial Lighting** (Bright Field) [redacted]			[redacted]

AS6171/3 X-RAY FLUORESCENCE (XRF) SPECTROSCOPY

TEST METHOD	REFERENCE / GOLDEN SAMPLE	DEVICE UNDER TEST (DUT #1)	COMPONENT ENGINEER COMMENTS
X-RAY FLUORESCENCE (XRF) SPECTROSCOPY [redacted]	  Meas. para. (foreground spectrum): High voltage = 50 kV (075) Prim. Filter = Ni10 Collimator 1 = 0.10 Dm. Anode current 1000 uA Meas. distance = -0.000 inch FastC = 285.58, SlowC = 284.13 List of spectra: Foreground: Measured spectrum	  Meas. para. (foreground spectrum): High voltage = 50 kV (075) Prim. Filter = Ni10 Collimator 1 = 0.10 Dm. Anode current 1000 uA Meas. distance = -0.000 inch FastC = 565.56, SlowC = 561.47 List of spectra: Foreground: Measured spectrum	[redacted]

	Sn ppm	Pb ppm	Ni ppm	Pd ppm	Cd ppm	Hg ppm
Mean	757114	3619.1	1687.3	2639.0	2582.3	6756.5
Standard Deviation	--------	--------	--------	--------	--------	--------
CoV (%)	0.00	0.00	0.00	0.00	0.00	0.00
Range	0.000	0.000	0.000	0.000	0.000	0.000
Number of readings	1	1	1	1	1	1
Tolerance Check	OL	OL	OL	OL	OL	OL

Measuring time: 20 sec

	Sn ppm	Pb ppm	Ni ppm	Pd ppm	Cd ppm	Hg ppm
Mean	206027	3623.4	79988	1723.2	5223.7	7449.9
Standard Deviation	--------	--------	--------	--------	--------	--------
CoV (%)	0.00	0.00	0.00	0.00	0.00	0.00
Range	0.000	0.000	0.000	0.000	0.000	0.000
Number of readings	1	1	1	1	1	1
Tolerance Check	OL	OL	OL	OL	OL	OL

Measuring time: 20 sec

AS6171A DEFINITIONS	
PART, ACTIVE, COMPLEX	An active device that contains multiple semiconductor junctions. Note: Examples include microcircuits such as microprocessors and memory devices.
PART, ACTIVE, SIMPLE	An active device that contains no more than a few semiconductor junctions. Note: Examples include diodes, transistors, and other discrete semiconductor devices.
AS6171/2 External Visual Inspection (EVI)	The EVI Inspection consists of a general inspection of the whole lot and a detailed Inspection of a selected sample of the lot. In the general EVI inspection, the complete lot of devices that are supplied to the Test Laboratory is inspected for possible signs of counterfeiting, including alterations of part marking, or alterations of paperwork supplied with the devices. The devices are optically examined at a suitable magnification and with suitable lighting per the EVI inspection procedure of this standard. The magnification used is dependent on the feature size that is being inspected. The Test Lab verifies that the part date and lot codes marked on the parts fall within the proper range of dates of manufacture (if such information is available).
AS6171/3 X-ray Fluorescence {XRF) Spectroscopy	A lead finish examination is performed on the sample devices that were examined for Remarking and Resurfacing, to verify that the Lead Finish/Solder Ball and Column composition matches the device specifications or datasheet.
AS6171/4 Delid/Decapsulation Physical Analysis (DDPA)	The primary purpose of DDPA is to verify that the die attributes are consistent with the known manufacturer of the device. Deviations from expected die attributes and internal construction may indicate a suspect counterfeit part.
AS6171/5 Radiological {X-ray) Inspection	The purpose of radiological inspection is to inspect the internal and external attributes of a part in order to detect deliberate misrepresentation or damage, which could indicate a suspect counterfeit part.
AS6171/6 Acoustic Microscopy	Acoustic Microscopy {AM) uses ultra-high frequency ultrasound to non-destructively find and characterize physical latent defects (visualization of interior features in a layer by layer

AS6171A DEFINITIONS	
	process) - such as material continuity, sub-surface flaws, cracks, voids, delaminations and porosity. AM observed features and defects can be indicators that the components were improperly handled, stored, altered or previously used, which could indicate a suspect/counterfeit part.
AS6171/7 Electrical	Electrical testing, if performed to the published electrical specifications, will determine whether the part operates in accordance with the part specifications. If not, any deviation from specifications could indicate a suspect/counterfeit part. This test method covers DC Curve Trace, Full DC Tests, Key Electrical Parameters for AC, Switching, and Functional Tests, both at ambient temperatures and over the parts full operating temperature range. The type of electrical test will be determined by the Risk Tier Level and part type as defined in 3.4, Suspect Counterfeit Part Detection Sequence of AS6171 General Requirements.
AS6171/8 Raman Spectroscopy	Raman spectroscopy is sensitive to vibrations within molecules and is used for identification of materials. A Raman spectrum is often compared to a "fingerprint" in that, at least in theory, all unique materials produce unique spectra.
AS6171/9 Fourier Transform Infrared (FTIR) Spectroscopy	Fourier Transform Infrared Spectroscopy is used to obtain infrared spectra of materials which are akin to "fingerprints" allowing for materials identification and verification. FTIR spectra are very similar to Raman spectra and interpretation is almost identical; a major exception being band intensities (strong bands in the infrared tend to be weak in the Raman and vice versa). Both Raman Spectroscopy and FTIR Spectroscopy are well-suited to detection of counterfeiting involving chemical or material modifications that are near a surface.
AS6171/10 Thermogravimetric Analysis (TGA)	Thermogravimetric Analysis (TGA) is a method in which the sample is exposed to a precisely controlled temperature environment while continuously monitoring weight change. The sample can be a liquid or a solid and weight change can be measured either during

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	controlled heating or while the sample is maintained at a constant temperature (isothermal period). Mass loss is equivalent to decomposition of constituents within the sample. Since decomposition occurs at unique temperatures, TGA can provide an indirect compositional analysis of the sample. This provides the ability to compare a DUT with an authentic part, or a materials specification, in order to make a compositional comparison of solid materials (e.g., plastic encapsulation from integrated circuits), or liquid materials (e.g., electrolyte saturated paper from within an electrolytic capacitor). TGA can also be used to analyze the composition of oils within a transformer or the volatilization of lubricants from a bearing. Additionally, it can be used to determine the moisture content of a polymer. This test method generally requires that a small portion of material be extracted and exposed to heat, which can be considered to be destructive. However, if an entire part is tested within its rated storage temperature range, the testing may be non-destructive.
AS6171/11 Design Recovery	Design Recovery is an in-depth, reverse engineering method to physically strip down a microcircuit or semiconductor device and recover design information. Depending on the test requirement this method can be very time consuming and requires a range of sample preparation, etch, metrology and imaging tools. If other test methods are being considered, depending on the requirements, those methods can be inserted into the Design Recovery procedure and carried out when appropriate. For example, if chemical analysis of the metallization used within an integrated circuit is required, EDS should be performed after the removal of the dielectric layer covering the metal layer and before the metal is removed. In the context of counterfeit detection this method could allow for the determination of whether the recovered design information of an IC matches the intended function or physical layout of an authentic part or matches the original design. This method can be applied to detecting tampered devices as well as unintentional changes in the IC's intended function from the physical layout of the circuit. This is a fundamentally destructive technique.